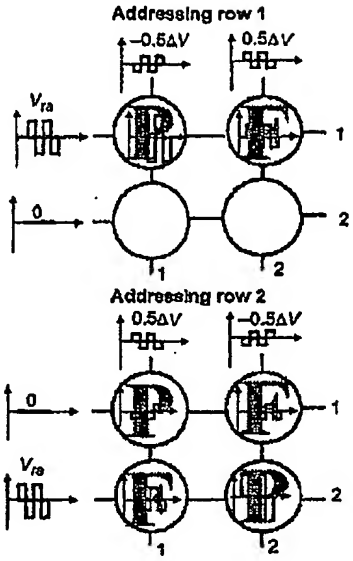

Figure 8.30 Schematic diagram showing the conventional drive scheme for the 2 × 2 bistable cholesteric display

Cholesteric (Ch) liquid crystal displays exhibit gray scale reflectance. In addressing a cholesteric display with gray scales, resetting is required, because the pulse voltage–reflectance curve depends on the initial state of the display, as shown in Figure 8.28. There are three schemes in addressing Ch displays with gray scale [30,41]. As an example, we consider the cholesteric display whose characteristic is shown in Figure 8.28. In the first scheme, gray scale is achieved using pulses with voltage in the region between V_1 and V_2. First, all the pixels are addressed into the planar texture by applying a high-voltage pulse. Then the display is addressed line by line as in the conventional drive scheme. The row voltage for the row being addressed is $V_a = (V_1 + V_2)/2$ and the row voltage for the rows not being addressed is 0. The column voltage is in the range from $-(V_2-V_1)/2$ to $(V_2-V_1)/2$. When the column voltage is $(V_2-V_1)/2$, the voltage across the pixel is

$$(V_1 + V_2)/2 - (V_2 - V_1)/2 = V_1$$

and the pixel remains in the planar texture with the maximum reflectance. When the column voltage is $-(V_2-V_1)/2$, the voltage across the pixel is

$$(V_1 + V_2)/2 - [-(V_2 - V_1)/2] = V_2$$

and the pixel is addressed completely into the focal conic texture with the minimum reflectance. When the column voltage is between $(V_2-V_1)/2$ and $-(V_2-V_1)/2$, the voltage

achieved. The time interval of the evolution phase can be chosen to be very long. The drive scheme even works well when the evolution time is as long as the frame time [66].

In the dynamic drive scheme, the time intervals of the preparation and evolution phases are long, typically more than 40 ms. This is, however, not a problem. The preparation and evolution times can be shared by putting multiple lines in these phases because the voltages are the same for all pixels, independent of the state to which the pixels will be addressed. This time-sharing pipeline algorithm is schematically shown in Figure 8.34. The column voltages are $V_4 = (V_{on} - V_{off})/2$ to select the off-state and $-V_4 = -(V_{on} - V_{off})/2$ to select the on-state, respectively, and have the frequency f_1. The row voltage for the preparation phase is V_1 which satisfies the relation $V_p = (V_1^2 + V_4^2)^{1/2}$, and has the frequency f_2 which is chosen to be very different from f_1. The number of lines put into the preparation phase is equal to or larger than $n_p = t_p/t_s$. The row voltage for the selection phase is V_2 which is equal to $(V_{on} + V_{off})/2$ and has the frequency f_1. Only one line is put into the selection phase. The voltage for the evolution phase is V_3 which satisfies the relation $V_e = (V_3^2 + V_4^2)^{1/2}$ and has the frequency f_2. The number of lines put into the selection phase is equal to or larger than $n_p = t_e/t_s$. The row voltage for the rows after addressing is 0, and therefore the voltage across the pixel in the rows is V_4 which does not cause cross-talk problems. Thus the frame time for an n-line display is given by

$$t_{frame} = t_p + t_e + n \times t_s \tag{8.58}$$

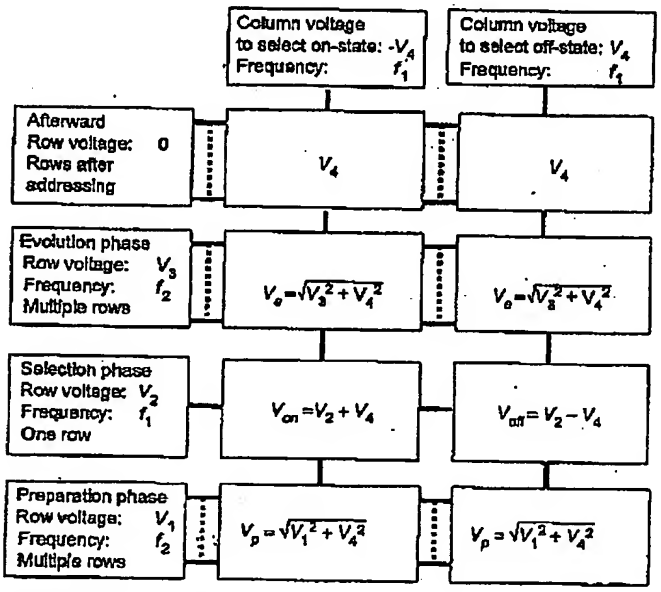

Figure 8.34 Schematic diagram showing how the cholesteric display is addressed in the dynamic drive scheme